AMENDMENTS TO THE SPECIFICATION

On page 4, please amend the paragraph beginning on line 9 as follows:

For writing data to the memory cell 100, a program voltage of about 12 V is applied to the control gate 107, a drain voltage of about 6 V is applied to the drain region 102, and a reference voltage of 0 V is applied to the source region 103 and the channel region in the semiconductor substrate 101 (as shown in figure 8).

On pages 25-26, please amend the paragraph beginning on page 25, line 22 as follows:

The memory array 50 includes a plurality of non-volatile semiconductor memory cells 10. The gate electrode 21 of each memory cell 10 is connected to the respective line of word lines WL00 through WL0n-l. The variable resistor 30 connected to the drain region 23 (as shown in figure 1) which is a driving region of each memory cell 10, is connected to the respective bit line of bit lines BL00 through BL0n-1. The memory cells 10 are arranged in a matrix.

On page 34, please amend the paragraph beginning on line 14 as follows:

Figure 4 is a flowchart illustrating a second data write method for writing data to the memory array 50 according to the present invention, as illustrated by steps S201-S215.

On page 41, please amend the paragraph beginning on line 1 as follows:

Figure 6 is a flowchart illustrating a fourth data write method four writing data to the memory array 50 according to the present invention, as illustrated by steps S401-S415.